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1 Procedure placement using temporal-ordering information

Nikolas Gloy, Michael D. Smith
September 1999 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 21 Issue 5
Publisher: ACM Press
Full text available: pdf(604.56 KB) Additional Information: full citation, abstract, references, citings, index terms

Instruction cache performance is important to instruction fetch efficiency and overall processor performance. The layout of an executable has a substantial effect on the cache miss rate and the instruction working set size during execution. This means that the performance of an executable can be improved by applying a code-placement algorithm that minimizes instruction cache conflicts and improves spatial locality. We describe an algorithm for procedure placement, one type of code placement ...

Keywords: code placement, conflict misses, temporal profiling, working-set optimization

2 Procedure placement using temporal ordering information

Nikolas Gloy, Trevor Blackwell, Michael D. Smith, Brad Calder
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture MICRO 30**
Publisher: IEEE Computer Society
Full text available: pdf(1.38 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Instruction cache performance is very important to instruction fetch efficiency and overall processor performance. The layout of an executable has a substantial effect on the cache miss rate during execution. This means that the performance of an executable can be improved significantly by applying a code-placement algorithm that minimizes instruction cache conflicts. We describe an algorithm for procedure placement, one type of code-placement algorithm, that significantly differs from previous ...

Keywords: code layout, conflict misses, profiling

3 Memory Protection through Dynamic Access Control

Kun Zhang, Tao Zhang, Santosh Pande
December 2006 **Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture MICRO 39**
Publisher: IEEE Computer Society
Full text available: pdf(274.63 KB) Additional Information: full citation, abstract, index terms

Current anomaly detection schemes focus on control flow monitoring. Recently, Chen et al. [2] discovered that a large category of attacks tamper program data but do not alter control flows. These attacks are not only realistic, but are also as important as classical attacks tampering control flows. Detecting these attacks is a critical issue but has received little attention so far. In this work, we propose an intrusion detection scheme with both compiler and micro-architecture support detecting ...

4 Programming languages: Compiler-assisted demand paging for embedded systems with flash memory
Chanik Park, Junghee Lim, Kiwon Kwon, Jaejin Lee, Sang Lyul Min
September 2004 **Proceedings of the 4th ACM international conference on Embedded software EMSOFT '04**
Publisher: ACM Press
Full text available: pdf(392.66 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we propose a novel, application specific demand paging mechanism for low-end embedded systems with flash memory as secondary storage. These systems are not equipped with virtual memory. A small memory space called an execution buffer is allocated to page an application. An application-specific page manager manages the buffer. The manager is generated by a compiler post-pass and combined with the application image. Our compiler post-pass analyzes the ELF executable image of an appl ...

Keywords: SRAM, clustering, compilers, embedded systems, flash memory, heterogeneous memory, paging, post-pass optimization

5 Shasta: a low overhead, software-only approach for supporting fine-grain shared memory
Daniel J. Scales, Kourosh Gharachorloo, Chandramohan A. Thekkath
October 1996 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 30 , 31 Issue 5 , 9
Publisher: ACM Press
Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes Shasta, a system that supports a shared address space in software on clusters of computers with physically distributed memory. A unique aspect of Shasta compared to most other software distributed shared memory systems is that shared data can be kept coherent at a fine granularity. In addition, the system allows the coherence granularity to vary across different shared data structures in a single application. Shasta implements the shared address space by transparently rewrit ...

6 Stored data structures on the Manchester dataflow machine
J. Sargeant, C. C. Kirkham
June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2
Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(676.26 KB) Additional Information: full citation, abstract, references, citings, index terms

Experience with the Manchester Dataflow Machine has highlighted the importance of efficient handling of stored data structures in a practical parallel machine. It has proved necessary to add a special-purpose structure store to the machine, and this paper describes the role of this structure store and the software which uses it. Some key issues in data structure handling for parallel machines are raised.

7 Microcomputer access to cross software systems

Bernard J. Carey, Anne-Marie G. Discepolo

September 1980 **Proceedings of the 3rd ACM SIGSMALL symposium and the first SIGPC symposium on Small systems SIGSMALL '80**

Publisher: ACM Press

Full text available: pdf(707.45 KB) Additional Information: full citation, abstract, references, index terms

Downline loading involves the transferral of information from the internal memory of one computer to the internal memory of another. For development microcomputer systems utilizing cross assemblers (i.e. non-resident assemblers), downline loading provides an extremely fast method of transferring cross-assembled files into the microprocessor's memory. The design for one low-cost method of linking a microcomputer system to a larger computer for downline loading is described. In this design, t ...

Keywords: Downline load, Microcomputer, Serial I/O

8 New twists on memory management: Reliability-aware data placement for partial memory protection in embedded processors

Mojtaba Mehrara, Todd Austin

October 2006 **Proceedings of the 2006 workshop on Memory system performance and correctness MSPC '06**

Publisher: ACM Press

Full text available: pdf(330.07 KB) Additional Information: full citation, abstract, references, index terms

Low cost protection of embedded systems against soft errors has recently become a major concern. This issue is even more critical in memory elements that are inherently more prone to transient faults. In this paper, we propose a reliability aware data placement technique in order to partially protect embedded memory systems. We show that by adopting this method instead of traditional placement schemes with complete memory protection, an acceptable level of fault tolerance can be achieved while i ...

Keywords: embedded systems, memory lifetime, partial memory protection, selective data placement, soft errors

9 Efficient indexing data structures for flash-based sensor devices

Song Lin, Demetrios Zeinalipour-Yazti, Vana Kalogeraki, Dimitrios Gunopulos, Walid A. Najjar

November 2006 **ACM Transactions on Storage (TOS)**, Volume 2 Issue 4

Publisher: ACM Press

Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, index terms

Flash memory is the most prevalent storage medium found on modern *wireless sensor devices (WSDs)*. In this article we present two external memory index structures for the efficient retrieval of records stored on the local flash memory of a WSD. Our index structures, *MicroHash* and *MicroGF (micro grid files)*, exploit the asymmetric read/write and wear characteristics of flash memory in order to offer high-performance indexing and searching capabilities in the presence of a low- ...

Keywords: Wireless sensor networks, access methods, flash memory

10 Hardware Support: Heads and tails: a variable-length instruction format supporting parallel fetch and decode

Heidi Pan, Krste Asanović
November 2001 **Proceedings of the 2001 international conference on Compilers, architecture, and synthesis for embedded systems CASES '01**
Publisher: ACM Press

Full text available: pdf(179.93 KB) Additional Information: full citation, abstract, references, citings, index terms

Existing variable-length instruction formats provide higher code densities than fixed-length formats, but are ill-suited to pipelined or parallel instruction fetch and decode. This paper presents a new variable-length instruction format that supports parallel fetch and decode of multiple instructions per cycle, allowing both high code density and rapid execution for high-performance embedded processors. In contrast to earlier schemes that store compressed variable-length instructions in main mem ...

11 Office-by-example: an integrated office system and database manager

Kyu-Young Whang, Art Ammann, Anthony Bolmarcich, Maria Hanrahan, Guy Hochgesang, Kuan-Tsae Huang, Al Khorasani, Ravi Krishnamurthy, Gary Sockut, Paula Sweeney, Vance Waddle, Moshé Zloof
October 1987 **ACM Transactions on Information Systems (TOIS)**, Volume 5 Issue 4
Publisher: ACM Press

Full text available: pdf(2.86 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Office-by-Example (OBE) is an integrated office information system that has been under development at IBM Research. OBE, an extension of Query-by-Example, supports various office features such as database tables, word processing, electronic mail, graphics, images, and so forth. These seemingly heterogeneous features are integrated through a language feature called example elements. Applications involving example elements are processed by the database manager, an integrated ...

12 Learning forth with modular forth

Paul Frenger
March 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 3
Publisher: ACM Press

Full text available: pdf(636.88 KB) Additional Information: full citation, citings, index terms

13 Packet types: abstract specification of network protocol messages

Peter J. McCann, Satish Chandra
August 2000 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, Technologies, Architectures, and Protocols for Computer Communication SIGCOMM '00**, Volume 30 Issue 4
Publisher: ACM Press

Full text available: pdf(435.48 KB) Additional Information: full citation, abstract, references, citings, index terms

In writing networking code, one is often faced with the task of interpreting a raw buffer according to a standardized packet format. This is needed, for example, when monitoring network traffic for specific kinds of packets, or when unmarshaling an incoming packet for protocol processing. In such cases, a programmer typically writes C code that

understands the grammar of a packet and that also performs any necessary byte-order and alignment adjustments. Because of the complexity of certain ...

14 Implementation of collective I/O in the Intel Paragon parallel file system: initial experiences

Rajesh Bordawekar

July 1997 **Proceedings of the 11th international conference on Supercomputing ICS '97**

Publisher: ACM Press

Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms

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1 A multi-user data flow architecture

F. J. Burkowski

May 1981 **Proceedings of the 8th annual symposium on Computer Architecture ISCA '81**

Publisher: IEEE Computer Society Press

Full text available: pdf(606.85 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the design of a prototype data flow machine that has memory management hardware in each memory block. This facility allows loading and deleting code that is produced by independent compilations. The first sections of the paper deal with the general architecture of the machine and the format specifications for the instruction cells, logical addresses, and switch packets. The paper concludes with a discussion of the mapping hardware used in the memory blocks. The results ...

2 The architecture of CASSM: A cellular system for non-numeric processing

George P. Copeland, G. J. Lipovski, Stanley Y.W. Su

December 1973 **ACM SIGARCH Computer Architecture News , Proceedings of the 1st annual symposium on Computer architecture ISCA '73**, Volume 2 Issue 4

Publisher: ACM Press

Full text available: pdf(857.69 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the architecture of a context-addressed cellular system for non-numeric information processing, using an inexpensive, large-capacity circulating memory device. The system allows data to be represented in a structure very close to the form as the user perceives it (information structure) and allows the search operations of high level queries to be implemented directly. The information structures currently used in existing information systems are described. Then the archit ...

3 Protecting C programs from attacks via invalid pointer dereferences

Suan Hsi Yong, Susan Horwitz

September 2003 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 9th European software engineering conference held jointly with 11th ACM SIGSOFT international symposium on Foundations of software engineering ESEC/FSE-11**, Volume 28 Issue 5

Publisher: ACM Press

Additional Information:

Full text available: pdf(526.15 KB) full citation, abstract, references, citings, index terms

Writes via unchecked pointer dereferences rank high among vulnerabilities most often exploited by malicious code. The most common attacks use an unchecked string copy to cause a buffer overrun, thereby overwriting the return address in the function's activation record. Then, when the function "returns", control is actually transferred to the attacker's code. Other attacks may overwrite function pointers, setjmp buffers, system-call arguments, or simply corrupt data to cause a denial of service.A ...

Keywords: buffer overrun, instrumentation, security, static analysis

4 Memory and instruction-set customization for real-time systems: A novel technique to use scratch-pad memory for stack management

Soyoung Park, Hae-woo Park, Soonhoi Ha

April 2007 **Proceedings of the conference on Design, automation and test in Europe DATE '07**

Publisher: ACM Press

Full text available: pdf(273.20 KB) Additional Information: full citation, abstract, references

Extensive work has been done for optimal management of scratch-pad memory (SPM) all assuming that the SPM is assigned a fixed address space. The main target objects to be placed on the SPM have been code and global memory since their sizes and locations are not changed dynamically. We propose a novel idea of dynamic address mapping of SPM with the assistance of memory management unit (MMU). It allows us to use SPM for stack management without architecture modification and complier assistance. ...

5 Draft report on requirements for a common prototyping system

R. P. Gabriel

March 1989 **ACM SIGPLAN Notices**, Volume 24 Issue 3

Publisher: ACM Press

Full text available: pdf(4.76 MB) Additional Information: full citation, citings, index terms

6 Memory organization and management for linked data structures

Hirotoshi Maegawa

April 1991 **Proceedings of the 19th annual conference on Computer Science CSC '91**

Publisher: ACM Press

Full text available: pdf(863.07 KB) Additional Information: full citation, references

7 Relational Database Systemsr

Won Kim

September 1979 **ACM Computing Surveys (CSUR)**, Volume 11 Issue 3

Publisher: ACM Press

Full text available: pdf(2.67 MB) Additional Information: full citation, references, citings, index terms

8 The design, implementation, and evaluation of adaptive code unloading for resource-constrained devices

Lingli Zhang, Chandra Krintz

June 2005 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 2

Issue 2
Publisher: ACM Press
Full text available: pdf(814.17 KB) Additional Information: full citation, abstract, references, index terms

Java Virtual Machines (JVMs) for resource-constrained devices, e.g., hand-helds and cell phones, commonly employ interpretation for program translation. However, compilers are able to produce significantly better code quality, and, hence, use device resources more efficiently than interpreters, since compilers can consider large sections of code concurrently and exploit optimization opportunities. Moreover, compilation-based systems store code for reuse by future invocations obviating the redund ...

Keywords: Code unloading, JIT, JVM, code-size reduction, resource-constrained devices

9 Operating and runtime systems for high-end computing systems: HPC-Colony: services and interfaces for very large systems
Sayantan Chakravorty, Celso L. Mendes, Laxmikant V. Kalé, Terry Jones, Andrew Tauferner, Todd Inglett, José Moreira
April 2006 **ACM SIGOPS Operating Systems Review**, Volume 40 Issue 2
Publisher: ACM Press
Full text available: pdf(437.39 KB) Additional Information: full citation, abstract, references, index terms

Traditional full-featured operating systems are known to have properties that limit the scalability of distributed memory parallel programs, the most common programming paradigm utilized in high end computing. Furthermore, as processor counts increase with the most capable systems, the necessary activity to manage the system becomes more of a burden. To make a general purpose operating system scale to such levels, new technology is required for parallel resource management and global system mana ...

10 Real-time convergence of Ada and Java™
Ben Brosgol, Brian Dobbing
September 2001 **ACM SIGAda Ada Letters , Proceedings of the 2001 annual ACM SIGAda international conference on Ada SIGAda '01**, Volume XXI Issue 4
Publisher: ACM Press
Full text available: pdf(191.98 KB) Additional Information: full citation, abstract, references, citings, index terms

Two independent recent efforts have defined extensions to the Java platform that intend to satisfy real-time requirements. This paper summarizes the major features of these efforts, compares them to each other and to Ada 95's Real-Time Annex, and argues that their convergence with Ada95 may serve to complement rather than compete with Ada in the real-time domain.

Keywords: Ada, Java, Real-Time, asynchrony, garbage collection, scheduling, threads

11 VAX vector architecture
Dileep Bhandarkar, Richard Brunner
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a
Publisher: ACM Press
Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

The VAX Architecture has been extended to include an integrated, register-based vector processor. This extension allows both high-end and low-end implementations and can be supported with only small changes by VAX/VMS and VAX/ULTRIX operating systems. The

extension is effectively exploited by the new vectorizing capabilities of VAX FORTRAN. Features of the VAX Vector Architecture and the design decisions which make it a consistent extension of the VAX Architecture are discussed.

12 Compilers 2: Compiler supported high-level abstractions for sparse disk-resident datasets

Renato Ferreira, Gagan Agrawal, Joel Saltz

June 2002 **Proceedings of the 16th international conference on Supercomputing ICS '02**

Publisher: ACM Press

Full text available: pdf(256.71 KB) Additional Information: full citation, abstract, references, citings, index terms

Processing and analyzing large volumes of data plays an increasingly important role in many domains of scientific research. The complexity and irregularity of datasets in many domains make the task of developing such processing applications tedious and error-prone.We propose use of high-level abstractions for hiding the irregularities in these datasets and enabling rapid development of correct data processing applications. We present two execution strategies and a set of compiler analysis techni ...

Keywords: data Intensive computing, data Parallel compilation, restructing compilers, sparse computations

13 University design contest: The design and implementation of a DVB receiving chip with PCI interface

Xu Ningyi, Li Shaohua, Yu Wei, He Guanghui, Zhang Hao, Luo Fei, Zhou Zucheng

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(330.37 KB) Additional Information: full citation, abstract, references

A DVB receiving chip with PCI interface for PC is presented. The chip supports DVB protocols and integrates useful interfaces, including I^2C, SmartCard and PCI. A card with this chip could change PC into digital TV terminal. The architecture of FPGA prototype system together with some main design issues is introduced. The experimental result shows that the chip could accomplish required functionalities.

14 Melange: creating a "functional" internet

Anil Madhavapeddy, Alex Ho, Tim Deegan, David Scott, Ripduman Sohan

March 2007 **ACM SIGOPS Operating Systems Review , Proceedings of the 2007 conference on EuroSys EuroSys '07**, Volume 41 Issue 3

Publisher: ACM Press

Full text available: pdf(760.25 KB) Additional Information: full citation, abstract, references

Most implementations of critical Internet protocols are written in type-unsafe languages such as C or C++ and are regularly vulnerable to serious security and reliability problems. Type-safe languages eliminate many errors but are not used to due to the perceived performance overheads.

We combine two techniques to eliminate this performance penalty in a practical fashion: strong static typing and generative meta-programming. Static typing eliminates run-time type information by checkin ...

15 Context and Location: MRM server: a context-aware and location-based mobile e-commerce server

Lai Jin, Tatsuo Miyazawa

September 2002 **Proceedings of the 2nd international workshop on Mobile commerce WMC '02**

Publisher: ACM Press

Full text available: pdf(458.89 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces a Mobile Resource Management (MRM) system for mobile E-commerce developed last year, mainly focusing on the server's implementation. The major advantages of the MRM are: (1) It provides location-based and context-aware services for mobile users. (2) It helps mobile E-commerce service providers (such as local advertisers) improve the effectiveness of their services, (for example through: better advertisements). (3) It improves real-time E-commerce services. In this paper, we ...

Keywords: agent, application paradigm, location-based/context-aware service, mobile e-commerce, system architecture

16 Applications: A graphical programming system for molecular motif search

Janina Reeder, Robert Giegerich

October 2006 **Proceedings of the 5th international conference on Generative programming and component engineering GPCE '06**

Publisher: ACM Press

Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, index terms

We describe a graphical programming system for a domain specific language in biosequence analysis. It supports the development of programs for RNA structure prediction and motif search, created by biologists with little or no programming skills. The system combines several programming paradigms in a productive way. It has a client - server architecture, with a transport layer in XML. The graphical front-end is implemented in the object-oriented paradigm (using Java). Graphics are compiled into a ...

Keywords: RNA structure, dynamic programming

17 Throughput analysis and configuration design of a shared-resource multiprocessor system: PUMPS

Faye A. Briggs, Michel Dubois, Kai Hwang

May 1981 **Proceedings of the 8th annual symposium on Computer Architecture ISCA '81**

Publisher: IEEE Computer Society Press

Full text available: pdf(697.81 KB) Additional Information: full citation, abstract, references, citings, index terms

A new concept of designing multiprocessors, which share not only memory but also specially chosen peripheral processors and VLSI functional units, is introduced in this paper. Queuing analysis is performed on the potential throughput of the Purdue multiprocessor system (PUMPS). Configuration design of the shared resource pool is demonstrated with a special PUMPS design for interactive image processing. The resource optimization techniques being developed can be also applied to configuration ...

18 Dynamic page placement to improve locality in CC-NUMA multiprocessors for TPC-C

Kenneth M. Wilson, Bob B. Aglietti

November 2001 **Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '01**

Publisher: ACM Press

Full text available: pdf(828.19 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of CC-NUMA multiprocessors complicates the placement of physical memory pages. Memory closest to a processor provides the best access time, but optimal memory page placement is a difficult problem with process movement, multiple processes requiring access to the same physical memory page, and application behavior changing over execution time. We use dynamic page placement to move memory pages where needed for the database benchmark TPC-C executing on a four node CC-NUMA multiprocessor. D ...

Keywords: CC-NUMA, TPC-C, dynamic page placement, migration, multiprocessor, replication

19 Generation of formatters for context-free languages

Mark van den Brand, Eelco Visser
January 1996 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 5 Issue 1
Publisher: ACM Press

Full text available: pdf(2.33 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Good documentation is important for the production of reusable and maintainable software. For the production of accurate documentation it is necessary that the original program text is not copied manually to obtain a typeset version. Apart from being tedious, this will invariably introduce errors. The production of tools that support the production of legible and accurate documentation is a software engineering challenge in itself. We present an algebraic approach to the generation of tools ...

Keywords: document preparation, program generators

20 Short papers 2: Testing in resource constrained execution environments

Gregory M. Kapfhammer, Mary Lou Soffa, Daniel Mosse
November 2005 **Proceedings of the 20th IEEE/ACM international Conference on Automated software engineering ASE '05**
Publisher: ACM Press

Full text available: pdf(196.83 KB) Additional Information: full citation, abstract, references, index terms

Software for resource constrained embedded devices is often implemented in the Java programming language because the Java compiler and virtual machine provide enhanced safety, portability, and the potential for run-time optimization. It is important to verify that a software application executes correctly in the environment in which it will normally execute, even if this environment is an embedded one that severely constrains memory resources. Testing can be used to isolate defects within and es ...

Keywords: code unloading, test suite execution

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1 Arts short poster session 2: Tabletop community: artwork for visualization of social interactions using a bipartite network

Noriyuki Fujimura, Satoshi Fujiyoshi, Tom Hope, Takuichi Nishimura

October 2006 **Proceedings of the 14th annual ACM international conference on Multimedia MULTIMEDIA '06**

Publisher: ACM Press

Full text available: pdf(4.82 MB) Additional Information: full citation, abstract, references, index terms

"Tabletop Community" is an artwork that records interactions among users around a table. The artwork also visualizes a social network of users from data that show these interactions; the piece can present that network to other users as well. Its theme is self-recognition, which emerges from social interactions with others in a human network. It is intended to offer experiences of looking back at a user's past interactions with others within the perspective of a group (social network) in a visual ...

Keywords: information visualization, social interaction, social network

2 Draft report on requirements for a common prototyping system

R. P. Gabriel

March 1989 **ACM SIGPLAN Notices**, Volume 24 Issue 3

Publisher: ACM Press

Full text available: pdf(4.76 MB) Additional Information: full citation, citings, index terms

3 Context and Location: MRM server: a context-aware and location-based mobile e-commerce server

Lai Jin, Tatsuo Miyazawa

September 2002 **Proceedings of the 2nd international workshop on Mobile commerce WMC '02**

Publisher: ACM Press

Full text available: pdf(458.89 KB) Additional Information: full citation, abstract, references, citings, index terms

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services for mobile users. (2) It helps mobile E-commerce service providers (such as local advertisers) improve the effectiveness of their services, (for example through: better advertisements). (3) It improves real-time E-commerce services. In this paper, we ...

Keywords: agent, application paradigm, location-based/context-aware service, mobile e-commerce, system architecture

4 University design contest: The design and implementation of a DVB receiving chip with PCI interface

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1 Instruction fetch and control flow: Power-efficient instruction delivery through trace reuse

Chengmo Yang, Alex Orailoglu

September 2006 **Proceedings of the 15th international conference on Parallel architectures and compilation techniques PACT '06**

Publisher: ACM Press

Full text available: pdf(260.98 KB) Additional Information: full citation, abstract, references, index terms

As power dissipation inexorably becomes the major bottleneck in system integration and reliability, the front-end instruction delivery path in a traditional out-of-order superscalar processor needs to deliver high application performance in an energy-effective manner. This challenge can be addressed by efficiently reusing the work of fetch and decode performed during preceding loop iterations and resident mostly within the processor itself. As a large percentage of the instructions currently und ...

Keywords: adaptive processor, instruction delivery, low-power design

2 Compiling nested data-parallel programs for shared-memory multiprocessors

Siddhartha Chatterjee

July 1993 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 15 Issue 3

Publisher: ACM Press

Full text available: pdf(4.17 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: compilers, data parallelism, shared-memory multiprocessors

3 $TCOL_{Ada}$ and the "middle end" of the PQCC Ada compiler

Benjamin M. Brosgol

November 1980 **ACM SIGPLAN Notices , Proceeding of the ACM-SIGPLAN symposium on Ada programming language SIGPLAN '80**, Volume 15 Issue 11

Publisher: ACM Press

Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references

A compiler is traditionally partitioned into a (mostly) machine independent Front End which performs lexical, syntactic, and semantic analysis, and a machine dependent Back End which performs optimization and code generation. In the Ada compiler being implemented at Carnegie-Mellon University in the PQCC project, it is useful to identify a set of phases occurring at the start of the Back End - i.e., "Middle End" - after semantic analysis but before optimization. These phases, known collectively ...

4 A preliminary architecture for a basic data-flow processor

Jack B. Dennis, David P. Misunas
December 1974 **ACM SIGARCH Computer Architecture News , Proceedings of the 2nd annual symposium on Computer architecture ISCA '75**, Volume 3 Issue 4
Publisher: ACM Press
Full text available: pdf(675.64 KB) Additional Information: full citation, abstract, references, citings

A processor is described which can achieve highly parallel execution of programs represented in data-flow form. The language implemented incorporates conditional and iteration mechanisms, and the processor is a step toward a practical data-flow processor for a Fortran-level data-flow language. The processor has a unique architecture which avoids the problems of processor switching and memory/processor interconnecion that usually limit the degree of realizable concurrent processing. The architect ...

5 Cycles to recycle: garbage collection to the IA-64

Richard L. Hudson, J. Elliot Moss, Sreenivas Subramoney, Weldon Washburn
October 2000 **ACM SIGPLAN Notices , Proceedings of the 2nd international symposium on Memory management ISMM '00**, Volume 36 Issue 1
Publisher: ACM Press
Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, citings, index terms

The IA-64, Intel's 64-bit instruction set architecture, exhibits a number of interesting architectural features. Here we consider those features as they relate to supporting garbage collection (GC). We aim to assist GC and compiler implementors by describing how one may exploit features of the IA-64. Along the way, we record some previously unpublished object scanning techniques, and offer novel ones for object allocation (suggesting some simple operating system support that would simplify it ...

6 A preliminary architecture for a basic data-flow processor

Jack B. Dennis, David P. Misunas
August 1998 **25 years of the international symposia on Computer architecture (selected papers) ISCA '98**
Publisher: ACM Press
Full text available: pdf(787.60 KB) Additional Information: full citation, references, citings, index terms

7 A parallel virtual machine for efficient scheme compilation

Marc Feeley, James S. Miller
May 1990 **Proceedings of the 1990 ACM conference on LISP and functional programming LFP '90**
Publisher: ACM Press
Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, citings, index terms

Programs compiled by Gambit, our Scheme compiler, achieve performance as much as twice that of the fastest available Scheme compilers. Gambit is easily ported, while retaining its high performance, through the use of a simple virtual machine (PVM). PVM allows a wide variety of machine-independent optimizations and it supports parallel computation based on the future construct. PVM conveys high-level information

bidirectionally between the machine-independent front end of the compiler and th ...

8 A structural view of the Cedar programming environment

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann
August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4
Publisher: ACM Press

Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

9 Relational Database Systemsr

Won Kim
September 1979 **ACM Computing Surveys (CSUR)**, Volume 11 Issue 3
Publisher: ACM Press

Full text available: pdf(2.67 MB) Additional Information: full citation, references, citings, index terms

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